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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,879	02/04/2002	Dale E. Gulick	2000.051700/TT4031	5870

23720 7590 01/05/2005

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EXAMINER	
DAMIANO, ANNE L	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,879	GULICK, DALE E.	
	Examiner	Art Unit	
	Anne L Damiano	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/25/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 22-60* is/are rejected.

7)☒ Claim(s) *19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 40-60 are rejected under 35 U.S.C. 102(b) as being Poisner by (6,012,154).

As in claims 40, 47 and 54, Poisner discloses a method comprising:

entering a system state in the computer system (starting of the computer);

resetting a watchdog timer on the integrated circuit (column 2: lines 31-34);

determining an expiration of the watchdog timer on the integrated circuit (column 2: line 66-column 3: line 3);

evaluating the system state in the computer system (interrupt handler investigating malfunction); (column 3: lines 21-40) and

determining a system error in the computer system (column 5: lines 10-14); and

responding to the system error by a microcontroller on the integrated circuit (column 3: lines 21-40 and 5: lines 10-14). (The processor responds to a system error by running the Interrupt Handler.)

As in claims 41, 48 and 55, Poisner discloses the method of claims 40, 47 and 54, wherein resetting the watchdog timer on the integrated circuit comprises resetting the watchdog timer on the integrated circuit in response to entering the system state in the computer system (column 2: lines 31-34, and lines 43-44) (In response to entering the system state of the computer being on, the watchdog times is reset. However, also, when the timer expires and the system is in a state of malfunction and interrupt handler is called, the timer is also reset.)

As in claims 42, 49 and 56, Poisner discloses the method of claims 40, 47 and 54, wherein evaluating the system state in the computer system comprises evaluating the system state in the computer system in response to determining the expiration of the watchdog timer on the integrated circuit (column 3: lines 21-40 and 5: lines 10-14). (When the timer expires, an interrupt is generated. When an interrupt causes the processor to execute the interrupt handler.)

As in claims 43, 50 and 57, Poisner discloses the method of claims 40, 47 and 54, further comprising: storing an indication of the system state (column 3: lines 56-62). (When a partial reset is called, due to the timer expiring, the system state information is retained.)

As in claims 44, 51 and 58, Poisner discloses the method of claims 43, 50 and 56, wherein storing the indication of the system state comprises storing the indication of the system state in a storage location on the integrated circuit (column 3: lines 62-67).

As in claims 45, 52 and 59, Poisner discloses the method of claims 43, 50 and 56, wherein storing the indication of the system state comprises storing the indication of the system state in response to entering the system state in the computer system (column 3: lines 56-67). (When the timer expires and a partial reset occurs, the indication of the system state is stored.)

As in claims 46, 53 and 60, Poisner discloses the method of claim 43, 50 and 56, wherein evaluating the system state in the computer system comprises reading the indication of the system state (column 3: lines 59-67). (When the computer is reset the indication of the system state is read.)

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5, 9-18, 22-31 and 35-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay et al. (2003/0028633).

As in claims 1, 14 and 27, Lindsay discloses a circuit, comprising:

a first bus interface logic (multi-protocol bus interface or NIC) for coupling to a first external bus;

a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over the first external bus (paragraphs 16, 20 and 37, figure 8: component 52); (ASF controller can be equivalent to a microcontroller. (paragraph 37).)and

a watchdog timer coupled to the microcontroller, wherein the watchdog timer is coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication to the microcontroller in response to an expiration of the watchdog timer (paragraphs 51). (When it is determined that the primary power has changed the system state from not operating to operating, the watchdog timer is enabled and reset. If the watchdog timer expires, the ASF controller will be indicated.)

As in claims 2, 15 and 28, Lindsay discloses the circuit of claims 1, 14 and 27, further comprising:

a second bus interface logic for coupling to a first internal bus (figure 8: SMBus and PCI bus), wherein data from the first

external bus is routable by the embedded Alert Standard Format management engine over

the first internal bus (Paragraphs 16-18 and Figure 8).

As in claims 3, 16 and 29, Lindsay discloses the circuit of claims 2, 15 and 28, further comprising:

an embedded Ethernet controller coupled to the first internal bus (paragraph 17).

As in claims 4, 17 and 30, Lindsay discloses the circuit of claims 3, 16 and 29, wherein the embedded Ethernet controller is configured to route the Alert Standard Format sensor data from the embedded Alert Standard Format management engine to an external management server (paragraph 44).

As in claims 5, 18 and 31, Lindsay discloses the circuit of claims 1, 14 and 27, wherein the indication provided to the microcontroller includes a microcontroller interrupt (PET) (paragraph.74, 75 and 115).

As in claims 9, 22 and 35, Lindsay discloses the circuit of claim 1, 14 and 27, wherein the reset input is provided to the watchdog timer by the microcontroller (paragraph 113: lines 1-3).

As in claims 10, 23 and 36, Lindsay discloses the circuit of claim 1, 14 and 27, wherein the reset input is provided to the watchdog timer from an external processor (paragraph 113: lines 3-6). (The NIC receives the start message from an external processor.)

As in claims 11, 24 and 37, Lindsay discloses the circuit of claim 1, 14 and 27, the integrated circuit of claim 1, further comprising: a register configured to store system status information (paragraph 46).

As in claims 12, 25 and 38, Lindsay discloses the circuit of claim 11, 24 and 37, wherein the microcontroller is further configured to read the system status information from the register in response to the indication (paragraph 46).

As in claims 13, 26 and 39, Lindsay discloses the circuit of claim 12, 25 and 38, wherein the microcontroller is further configured to provide the system status information to an external management server (paragraph 74).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1, 2, 3 and 6-13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2, 3, 5 and 8-15 of copending Application No. 10/067,175 ('175 hereafter). Although the conflicting claims are not identical, they are not patentably distinct from each other because '175 claim 2 contains every limitation of instant application, excluding obvious variations.

These are a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding instant claim 1, '175 claim 2 claims every limitation besides, "a first bus interface logic" of instant claim 1, line 2 and "a watchdog timer coupled to the microcontroller" or instant claim 1, line 6.

'175 claim 2, contains logic to receive data over a first external bus (paraphrased from '175 claim 2.) Therefore, it is obvious that '175 claim 2, contains bus interface logic for coupling to the first external bus.

'175 claim 2 contains logic configured to query the watchdog timer, the logic comprising a microcontroller. Therefore, it is obvious that the watchdog timer of '175 claim 2 is in some way, coupled to the microcontroller.

'175 claim 2, includes logic configured to query the watchdog timer for the expiration of the watchdog timer which is not included in instant application claim 1. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well settled

that the omission of an element and it's function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA 1963).

Regarding instant claim 2 and '175 claim 3, both claim a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

Regarding instant claim 3 and '175 claim 5, both claim an embedded Ethernet controller coupled to the first internal bus.

Regarding instant claim 6 and '175 claim 8, both claim a bridge, wherein the bridge further comprises: a third interface logic for coupling to a second external bus.

Regarding instant claim 7 and '175 claim 9, both claim the bridge comprising a south bridge, wherein the first external bus is configurable as a first input/output bus.

Regarding instant claim 8 and '175 claim 10, both claim the first input/output bus being an SMB bus.

Regarding instant claim 9 and '175 claim 11, both claim the reset input being provided to the watchdog timer by the microcontroller.

Regarding instant claim 10 and '175 claim 12, both claim the reset input being provided to the watchdog timer from an external processor.

Regarding instant claim 11 and '175 claim 13, both claim a register configure to store system status information.

Regarding instant claim 12 and '175 claim 14, both claim the microcontroller being further configured to read the system status information from the register in response to the indication.

Regarding instant claim 13 and '175 claim 15, both claim the microcontroller being further configured to provide the system status information to an external management server.

8. Claim 27-29, 32-34, 36 and 37 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 30, 32, 34, 36, 37, 38, 40 and 41 of copending Application No. '175. Although the conflicting claims are not identical, they are not patentably distinct from each other because '175 claim 30 contains every limitation of instant application claim 27 with '175 including an additional limitation. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well settled that the omission of an element and it's function is an obvious expedient if the

remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA 1963).

These are a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding instant claim 27, every limitation of instant claim 27 is included in '175 claim 30. However, instant claim 27 does not teach logic being configured to query the watchdog timer for the expiration of the watchdog timer in response to receiving the request for the system reset is recited in '175 claim 31.

Applicant has clearly removed a function of the computer system as an obvious expedient.

Regarding instant claim 28 and '175 claim 32, both claim a second bus interface logic for coupling to a first internal bus, wherein data from the first external bus is routable by the embedded Alert Standard Format management engine over the first internal bus.

Regarding instant claim 29 and '175 claim 34, both claim an embedded Ethernet controller coupled to the first internal bus.

Regarding instant claim 32 and '175 claim 36, both claim the bridge further comprising: a third bus interface for coupling to the second external bus.

Regarding instant claim 33 and '175 claim 37, both claim the bridge comprising a south bridge, and wherein the first external bus is configured as a first input/output bus.

Regarding instant claim 34 and '175 claim 38, both claim the first input/output bus being an SMBus.

Regarding instant claim 36 and '175 claim 40, both claim a processor configured to provide the reset input to the watchdog timer.

Regarding instant claim 37 and '175 claim 41, both claim a register configure to store system status information.

Response to Arguments

9. Applicant's arguments with respect to claims 40-60 are not persuasive.

In response to applicant's arguments, the recitation "an integrated circuit, comprising:" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the

preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

10. Applicant's arguments with respect to claims 1-5, 9-18, 22-31 and 35-39 are not persuasive.

Firstly, the ASF controller is functionally equivalent to a microcontroller. See above claim rejections.

Secondly, in response to applicant's arguments, the recitation "an integrated circuit, comprising:" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Applicant's arguments with respect to the rejection(s)of claim(s) 6-8, 19-21 and 32-34 under Lindsay in view of AAPA have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made with respect to claims 6-8 and 32-34, in view of copending Application No. 10/067,175.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER